



FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 95-0653	Serial No: 08/650,719
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b)) (use several sheets if necessary)		Applicant: Mailloux et al.	
		Filing Date: 5/20/96	Group: 2511

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
UK	AA 5,357,469	10/18/94	Sommer et al.	✓ 365	193	
↑	AB 5,268,865	12/7/93	Takasugi	✓ 365	189.5	
	AC 4,618,947	10/21/86	Tran et al.	✓ 365	230.236	
	AD 5,267,200	11/30/93	Tobita	✓ 365	189.5 189.05	
	AE 4,344,156	8/10/82	Eaton et al.	✓ 365	203.189.05	
	AF 4,707,811	11/17/87	Takemae et al.	✓ 365	239	
	AG 4,649,522	3/10/87	Kirsch	✓ 365	189.05	
	AH 4,603,403	7/29/86	Toda	✓ 365	189.05	
	AI 4,567,579	1/28/86	Patel et al.	✓ 365	189.05	
↓	AJ 4,484,308	11/20/84	Lewandowski et al.	✓ 365 711	200 109	
UK	AK 4,875,192	10/17/89	Matsumoto	✓ 365	193	

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FOREIGN PATENT DOCUMENTS

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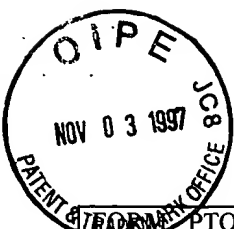
Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

UK	AR		Samsung Electronics, "Samsung Synchronous DRAM", March 1993, pgs. 1-16
UK	AS		Oki Electric Ind. Co., Ltd., "Burst DRAM Function & Pinout", 2nd presentation, Item #619, September, 1994
UK	AT		Toshiba, "Pipelined Burst DRAM", December 1994, JEDEC JC-42.3 Hawaii

Examiner: <i>UK</i>	Date Considered: <i>8/9/98</i>
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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
Wh	AA	4,685,089	8/4/87	Patel et al.	✓ 365	233 189.05
Wh	AB	4,562,555	12/31/85	Ouchi et al.	✓ 365	233 189.03
Wh	AC	4,575,825	3/11/86	Ozaki et al.	✓ 365	189 193
Wh	AD	4,788,667	11/29/88	Nakano	✓ 365	193
Wh	AE	5,392,239	2/21/95	Margulis et al.	✓ 365	189.01
Wh	AF	5,379,261	1/3/95	Jones, Jr.	✓ 365	230.01
Wh	AG	5,126,975	6/30/92	Handy et al.	✓ 365	230.01
Wh	AH	5,331,593	7/94	Merritt	✓ 365	189.11
Wh	AI	5,311,471	5/90	Matsumoto	✓ 365	189.05
Wh	AJ	5,526,320	6/11/96	Zagar et al.	✓ 365	233.5

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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

Wh	AR		Toshiba America Electronic Components, Inc., "Application Specific DRAM, 1994", Pgs. C-178, C-260, C218
Wh	AS		Micron Semiconductor, Inc., "Synchronous DRAM 2 MEG x 8 SDRAM", Pgs. 2-3 through 2-6, Rev. 4/94
Wh	AT		Toshiba America Electronic Components, Inc., "4M DRAM 1991", Pgs. A-137 - A-159

Examiner: <i>Wh</i>	Date Considered: <i>8/9/98</i>
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Examiner Initial	Document Number	Date	Name	Class	Subclass	
Wh	AA 5,268,865	12/93	Takasugi	✓ 365	189.05	
Wh	AB 5,319,759	6/94	Chan	✓ 365-711	230.08217	
Wh	AC 5,327,390	7/94	Takasugi	✓ 365	230.08	230.06
Wh	AD 5,426,606	6/95	Takai	✓ 365	230.06	189.05
Wh	AE 5,369,622	11/94	McLaury	✓ 365	233	
Wh	AF 5,568,445	10/96	Park et al.	✓ 365	233	
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OTHER ART (including author, title, date, pertinent pages, etc.)

Wh	AR		Micron Semiconductor, Inc., "1994 DRAM Data Book", pgs. 2-1 to 2-6
Wh	AS		Mosel-Vitelc V53C8257H DRAM Specification Sheet, 20 pgs. Rev. 02 July 1994
Wh	AT		Toshiba Corp., "Integrated Circuit Technical Data-262,144 Words x 8 Bits Multiport DRAM", TC52826TS/Z/FT/TR, TEN. Rev. 2.1 Date is missing

Examiner: <i>Wh</i>	Date Considered: <i>8/9/98</i>
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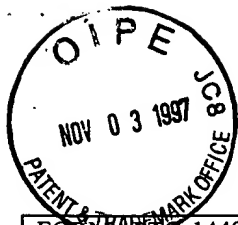
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OTHER ART (including author, title, date, pertinent pages, etc.)

<i>Wk</i>	AR		Micron Technology, Inc., "Burst EDO DRAM Information", pgs. 1-126, Rev. 9/95
<i>Wk</i>	AS		NEC "Command Truth Table" March 15, 1993
<i>Wk</i>	AT		Samsung Electronics "KM48SV2000 Preliminary CMOS SDRAM" Rev.1(Mar, 1993), pgs. 7-8

Examiner: <i>Wk</i>	Date Considered: <i>8/9/98</i>
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<i>Wk</i>	AR		"Hyper Page Mode DRAM", 8029 Electronic Engineering, 66, No. 813, Woolwich, London, GB, pp. 47-48, (September 1994)
<i>Wk</i>	AS		Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)
<i>Wk</i>	AT		Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode Access", IEEE, Cusom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)

Examiner: <i>H Kiri</i>	Date Considered: <i>8/9/98</i>
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Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

<i>DL</i>	AR		S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages
<i>Wk</i>	AS		Electronic News "Mitsubishi Samples 16M Synch DRAM", 10/25/93, pgs. 3-4
<i>Wk</i>	AT		"DRAM 1 Meg X 4 DRAM 5BEDO Page Mode", 1995 DRAM Data Book, pp.1-1 thru 1-30,, (Micron Technology, I)

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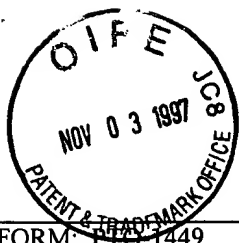
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uk	AR		Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)	Suplicant	3/12/99
uk	AS		Access", IEEE, Custom Integrated Circuits Conference, pp. 781-786, (March 3, 1992)	Suplicant	3/12/99
1	AT				

Examiner: H. Kim	Date Considered: 8/9/98
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uk	AR		Micron Semiconductor, Inc., "Synchronous DRAM 4 Meg x 4 SDRAM", Pgs. 2-1 to 2-2 "1994 DRAM DATA BOOK" 5/13/99
uk	AS		Micron Technology, Inc., "1996 DRAM Data Book", Pgs. 1-1 to 1-52, and 4-1 to 4-42
uk	AT		Micron Technology, Inc., "1995 DRAM Data Book", Pgs. 3-1 to 3-37

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